	DPG Institute of Technology and Management **Sector 34, Gurugram HR 122004**
	Lesson Plan
	Course Name: B.TECH (ECE)
	Faculty Name: Archana Rohilla (Assistant Professor)

No. of Lecture Hours/Week		**Exam Hours**	**3**
Total No. of Lecture Hours		**Exam Marks**	**75**
Course Code:	**PCC-ECE-303G**	**SEMESTER**	**5th**

Course Objectives:

1. How Computer Systems work & the basic principles
2. Instruction Level Architecture and Instruction Execution
3. The current state of art in memory system design
4.How I/O devices are accessed and its principles.
5.To provide the knowledge on Instruction Level Parallelism
6.To impart the knowledge on micro programming
7 Concepts of advanced pipelining techniques.

Lecture No.	Topics to be covered	Teaching Methodology	Class Activity/ Event	Remark /CO
SECTION A				**CO1**
1	Data Types, Complements, Fixed-Point Representation	Chalk &Talk		
2	Conversion of Fractions, Floating-Point Representation,	Chalk &Talk		
3	Gray codes, Decimal codes, Alphanumeric codes, Error Detection Codes.	Chalk &Talk	ASSIGNMENT-1	
4	Register Transfer Language, Register Transfer	SMART BOARD		
5	Bus and Memory Transfer, Arithmetic Microoperations, Logic Microoperations	Chalk &Talk		
6	Shift Microoperations, Arithmetic Logic Shift Unit.			

SECTION B				**CO2**
7	Instruction Codes, Computer Registers, Computer Instructions	Chalk &Talk		
8	Timing and Control, Instruction Cycle	Chalk &Talk		
9	Memory-Reference Instruction, Input-Output Instruction	SMART BOARD		
10	Complete Computer Description, Design of Basic Computer	Chalk &Talk		
11	Design of Accumulator Logic.			
12	General Register Organization, Stack organization	Chalk &Talk		
13	Instruction Format, Addressing Modes	Chalk &Talk		
14	Data Transfer and Manipulation, Program Control, RISC, CISC.	Chalk &Talk		
SECTION C				**CO3**
15	Parallel Processing, Amdahl's law	Chalk &Talk		
16	Pipelining, Arithmetic Pipeline		ASSIGNMENT-2	
17	Instruction Pipeline, Pipeline Hazards, RISC Pipeline.	Chalk &Talk		
18	Introduction to Parallel Processors	Chalk &Talk		
19	Arithmetic Pipeline, Instruction Pipeline, Pipeline Hazards, RISC Pipeline.	Chalk &Talk		
20	Vector Operations, Memory Interleaving	PPT		
21	Supercomputers, Array Processors: Attached Array Processor	PPT		

22	SIMD Array Processor.	Chalk &Talk		
SECTION D				**CO4**
23	I/O device interface, I/O transfers–program controlled	Chalk &Talk		
24	interrupt driven and DMA,	Chalk &Talk		
25	Privileged and Non-Privileged Instructions, Software Interrupts	PPT		
26	Memory Hierarchy, Main Memory, Auxiliary Memory	Chalk &Talk		
27	Associative Memory, Cache Memory	Chalk &Talk		
28	Associative Mapping, Direct Mapping, Set-Associative Mapping	Chalk &Talk		
32	Writing into Cache, Cache Initialization, Virtual Memory.	PPT		

Suggested Test books:

1) "Computer System Architecture", 3rd Edition by M.Morris Mano, Pearson.
2) "Computer Organization and Design: The Hardware/Software Interface", 5th Edition by David A. Patterson and John L. Hennessy, Elsevier.
3) "Computer Organization and Embedded Systems", 6th Edition by CarlHamacher, McGraw Hill Higher Education

Course Outcomes:

At the end of the course, the student will be able:

CO 1	Draw the functional block diagram of a single bus architecture of a computer and describe the function of the instruction execution cycle, RTL interpretation of instructions, addressing modes, instruction set.
CO 2	Write assembly language program for specified microprocessor for computing 16 bit multiplication, division and I/O device interface (ADC, Control circuit, serial port communication).
CO 3	Write a flowchart for Concurrent access to memory and cache coherency in Parallel processors and describe the process.
CO 4	Given a CPU organization and instruction, design a memory module and analyze its operation by interfacing with the CPU. Given a CPU organization, assess its

	performance, and apply design techniques to enhance performance using pipelining, parallelism and RISC methodology.