DPG Institute of Technology and Management
Sector 34, Gurugram HR 122004

Lesson Plan

Course Name: DIGITAL ELECTRONICS

Faculty Name: RICHA NEHRA

No. of Lecture Hours/Week	**3**	**Exam Hours**	**3**
Total No. of Lecture Hours	**40**	**Exam Marks**	**75**
Course Code:	**PCC-CSE-205G**	**Semester**	**3rd**

Course Objectives:

1. Understand working of logic families and logic gates.
2. Design and implement Combinational logic circuits.
3. Design and implement Sequential logic circuits.
4. Understand the process of Analog to Digital conversion and Digital to Analog conversion. Use PLDs to implement the given logical problem.

Lecture No.	Topics to be covered	Teaching Methodology	Class Activity/ Event	Remark /CO
UNIT -1				
1	Introduction to Digital & Analog Signals, Digital Circuits	Chalk &Talk		CO1
2	AND, OR, NOT Gates – Truth Tables & Realization	Chalk &Talk		
3	NAND, NOR, XOR, XNOR Gates & Universal Gate Concept	PPT/Chalk &Talk	Problem-solving session	
4	Boolean Algebra – Rules, De Morgan's Theorems	Chalk &Talk	Demonstration using tables	
5	Number Systems – Binary, Octal, Hexadecimal Conversions	Chalk &Talk		
6	Signed Binary, 1's and 2's Complement Arithmetic	Chalk &Talk		
7	Binary Addition & Subtraction – Half & Full Concept Review	Chalk &Talk	Board derivations	
8	Codes – BCD, Gray Code, Excess-3, ASCII	Chalk &Talk	Practice K-map problems	
9	Error Detecting & Correcting Codes (Parity, Hamming Code)	Chalk &Talk		
10	**Unit-I Review + Assignment / Test**	Chalk &Talk		

UNIT -2				
11	Representation of Logic Functions, SOP & POS Forms	Chalk &Talk		CO2
12	K-Map (2, 3 & 4 Variables) Simplification	Chalk &Talk		
13	Don't Care Conditions & Minimization Examples	Chalk &Talk		
14	Multiplexer & Demultiplexer – Design Examples	Chalk &Talk		
15	Encoders, Decoders, Priority Encoders	Chalk &Talk		
16	Adders, Subtractors, BCD Adder, Carry Look Ahead Adder	Chalk &Talk		
17	Digital Comparator, Parity Generator/Checker, Code Converters	Chalk &Talk		
18	ALU Concept & MSI Chips	Discussion		
19	Q-M Method of Logic Realization			
20	**Unit-II Review + Short Test**			
UNIT -3				
21	1-Bit Memory & Bistable Latch Operation	Chalk &Talk		CO3
22	Clocked SR Flip-Flop – Truth Table, Excitation Table	PPT		
23	JK, D & T Flip-Flops – Conversions	PPT		
24	Applications of Flip-Flops	SMART BOARD		
25	Shift Registers (SISO, SIPO, PISO, PIPO)	SMART BOARD		
26	Ring Counter, Johnson Counter	Chalk &Talk		
27	Parallel to Serial & Serial to Parallel Converters	Chalk &Talk		
28	Ripple Counters (Asynchronous)	Discussion		
29	Synchronous Counters & Design using Flip-Flops			
30	Special Counter ICs (7490, 74192 etc.)			
31	Sequence Generators			
32	**Unit-III Review**		Assessment activity	
UNIT -4				
33	D/A Converters – Weighted Resistor & R-2R Ladder	Chalk &Talk	Block diagram discussion	

34	D/A Specifications & Example ICs	SMART BOARD	Block diagram discussion	CO4
35	Sample and Hold Circuit	Chalk &Talk		
36	A/D Converters – Quantization & Encoding; Flash ADC	Chalk &Talk		
37	Successive Approximation, Dual Slope, Counting ADCs	Chalk &Talk		
38	Memory Organization & Types (ROM, RAM, CAM)	Chalk &Talk		
39	PLD, PLA, PAL, CPLD, FPGA Concepts	Chalk &Talk		
40	**Unit-IV Review + Model Exam**		Mock test / viva	

Assessment Methods: -

S.No.	Evaluation Component	Assessment Method	Marks
1	**Internal Marks**		**25**
		Attendance	**5**
2		**Quiz/Presentation**	**5**
3		**Assignment**	**5**
4		**Avg of Sessional 1&2**	**10**
5	**External Marks**	**Final University Exam**	**75**

Reference Books:

1.R. P. Jain, "Modern DigitalElectronics",McGrawHillEducation, 2009.

2. M. M.Mano, "Digital logic and Computerdesign",Pearson Education India,2016.

3. A. Kumar,"Fundamentals ofDigitalCircuits",Prentice HallIndia, 2016.

4. Nasib Singh Gill and J B Dixit, “Digital Design and Computer Organization”, University Science Press, New Delhi

Course Outcomes:

At the end of the course, the student will be able:

CO 1	Understand working of logic families and logic gates.
CO 2	Design and implement Combinational and Sequential logic circuits.
CO 3	Understand the process of Analog to Digital conversion and Digital to Analog conversion.
CO 4	Use PLDs to implement the given logical problem.